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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,088	01/29/2004	Andrew T. Tomerlin	CML01079J	4603

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MOTOROLA, INC
INTELLECTUAL PROPERTY SECTION
LAW DEPT
8000 WEST SUNRISE BLVD
FT LAUDERDAL, FL 33322

EXAMINER	
LUU, AN T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/767,088	TOMERLIN ET AL.	
	Examiner	Art Unit	
	An T. Luu	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21 and 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21,29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's Amendment filed on 8-31-05 has been received and entered in the case. The rejections set forth in the previous Office Action are maintained as indicated below.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6-10 and 17-21 are rejected under 35 U.S.C. 102(b) as being anticipated by the Yokota et al reference (U.S. Patent 5,712,582).

Yokota et al discloses in figure 1 an apparatus comprising a variable length delay line 100, the delay line having an input and having N delay elements (D1-m) to provide a plurality of N delayed outputs as shown; the variable length delay line having a number of active delay elements determined by a program command (select signal); and a configurable processing array 130 receiving the delayed outputs from the active delay elements and secondary processing data (delay data), the configurable processing array comprising an array of configurable circuit elements (G1-m) as required by claim 1.

As to claim 2, figure 1 shows a control processor 160 that configures the number of active delay elements of the variable length delay line and configures the array of configurable circuit elements.

As to claim 3, figure 1 shows a control processor 160 controlling the delay of the N delay elements.

As to claim 4,figure 1 shows a delay locked loop 100 controlling the delay of the N delay elements.

As to claim 6, figure 1 shows the configurable processing array comprising an input (output of 400) and output (output of OR gate) that can be configured under a program control (selector control and decoder 160).

As to claim 7, figure 1 shows the configurable processing array comprising a plurality of outputs (output of G1-m) that can be configured under a program control (selector control and decoder 160).

As to claim 8, figure 1 shows the apparatus comprising a plurality of configurable processing unit (G1-m).

As to claim 9, figure 1 shows the apparatus comprising a programmable logic device 160.

As to claim 10, the apparatus comprising a programmable MUX (i.e., decoder 160) responsive to a command (delay data) to selectively enable a selected group of delay elements while disabling remaining delay elements (i.e., which tap output is selected).

As to claims 17-21, they are rejected for reciting method/step derived from the apparatus of claims 1, 2, 3, 6, 8 and 9 which are rejected as noted above.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 11-16 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Yokota et al reference (U. S. Patent 5,712,58) in view of the Lee reference (U.S. Patent 5,901,190).

Yokota et al discloses all the claimed invention except for disclosing a delay element comprising a pair of series connected inverters as required by claims 5, 25 and 28.

Lee discloses in figure 4 a delay line comprising delay elements having a pair of series connected inverters (FUD1-n) as required by the claims.

It would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching of Lee into that of Yokota and to realize the delay as two series connected inverters.

A skilled artisan would be motivated to employ such to provide a minimized phase difference between tapped outputs.

As to claim 11, the scope of claim is similar to the combination of claims 1, 2, 4 and 5. Therefore, it is rejected for the same reason set forth above.

As to claim 12, the scope of claim is similar to the combination of claims 1, 2, 4, 5 and 6. Therefore, it is rejected for the same reason set forth above.

As to claim 13, the scope of claim is similar to the combination of claims 1, 2, 4, 5 and 7. Therefore, it is rejected for the same reason set forth above.

As to claim 14, the scope of claim is similar to the combination of claims 1, 2, 4, 5 and 8. Therefore, it is rejected for the same reason set forth above.

As to claim 15, the scope of claim is similar to the combination of claims 1, 2, 4, 5 and 9. Therefore, it is rejected for the same reason set forth above.

As to claim 16, the scope of claim is similar to the combination of claims 1, 2, 4, 5 and 10. Therefore, it is rejected for the same reason set forth above.

As to claim 29, the scope of claim is similar to the combination of claims 11, 12, 13 and 14. Therefore, it is rejected for the same reasons set forth above.

Response to Arguments

5. Applicant's arguments filed 8-31-05 have been fully considered but they are not persuasive.

Regarding the rejections of claims under 35 USC 102, Applicant has argued that element 130 of Yokota is not "a configurable processing array" as defined in page 4 of Applicant's specification. Examiner respectfully disagrees. In a broad reasonable interpretation, a selector circuit 130, as disclosed in Yokota, can be seen as a configurable processing array since it is a programmable logic device having plurality of logic gates which are programmed by controller 160. Therefore, the limitation "a configurable processing array" is clearly anticipated by selector 30 of Yokota.

Applicant further argues that the delay line 120 of Yokota is fixed in length wherein claim 1 calls for a variable length delay line. Examiner respectfully disagrees. The length of delay of Yokota is determined by a number of active AND circuits (i.e., number of active delay units of the delay line). Therefore, Yokota's delay line is a variable delay line. It is noted that the variable delay line 120 of Yokota is identically configured as each and every delay line shown in drawings of the instant application.

Regarding the rejection of claims under 35 USC 103, Applicant has argued that there is no prima facie obviousness since the primary reference does not teach all the claimed limitations in the independent claims (i.e., a configurable processing array, variable length delay). Applicant's argument is moot since the rejection of the independent claims is based on a combination of prior art and addresses each and every limitations required by the claims.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
10-12-05 ATL

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800